ABSTRACT

In this invention a stacked gate flash memory cell is disclosed which has a lightly doped drain (LDD) on the drain side of the device and uses the source to both program using hot electron generation and erase the floating gate using Fowler-Nordheim tunneling. Disturb conditions are reduced by taking advantage of the LDD and the biasing of the cell that uses the source for both programming and erasure. The electric field of the drain is greatly reduced as a result of the LDD which reduces hot electron generation. The LDD also helps reduce bit line disturb conditions during programming. A transient bit line disturb condition in a non-selected cell is minimized by preconditioning the bit line to the non-selected cell to Vcc.